

**REMARKS**

**I. Status of Application**

By the present Amendment, claims 1 and 3 have been amended and new claims 30-35 have been added. Claims 1-3, 6-7, 10-11, 14, 18-26, 29 and 30-35 are all the claims pending in the application. Claims 1-3, 18, 19, 22 and 29 have been rejected.

**II. Allowable Subject Matter**

Claims 6, 7, 10, 11, 14, 20, 21 and 23-26 are all the claims allowed.

**III. Formalities**

Applicant again respectfully reminds the Examiner that he has not provided a signed Form 1449 (SB08) for the IDS submitted on March 14, 2008. Applicant respectfully requests that the Examiner kindly indicate that the IDS has been considered by providing a signed Form 1449 (SB08) with the next office action.

**IV. Objections to the Drawings**

The Examiner has objected to the Drawings, alleging that the recitation of “a plurality of stacked inverter stages” as recited in claim 19 must be shown in the drawings or canceled from the claims. Applicant respectfully traverses these objections.

As set forth in the Statement of Substance of Interviews filed on October 13, 2009, to address these objections, a telephone interview was initiated by Applicant’s representative on October 6, 2009. During the interview, Applicant’s representative explained that the outstanding Objections to the Drawings set forth in the June 8, 2009 Office Action were improper because *at least* FIG. 9 of the originally filed specification adequately shows the features recited in claim 19, as described on page 19, lines 18-25 of the original specification. In response, the Examiner

agreed to consider such arguments and to telephone Applicant's representative once the Examiner had determined whether such arguments overcome the outstanding Objections to the Drawings.

On October 7, 2009, Applicant's representative received a return call from the Examiner confirming that arguments that *at least* FIG. 9 of the originally filed specification adequately shows the features recited in claim 19, as described on page 19, lines 18-25 of the original specification, overcome the outstanding Objections to the Drawings.

In view of the above, Applicant respectfully requests that the Examiner withdraw these objections.

**V. Claim Rejections Under 35 U.S.C. § 102**

Claims 1-3, 18, 19 and 29 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Uchida (US 5,926,046). Applicant respectfully traverses these rejections.

First, as acknowledged by the Examiner in the 10/16/08 Office Action, and the interviews conducted on December 30 and 31, 2008, previous claims 27 and 28 (claims 27 and 28 were previously incorporated into claims 1 and 3, respectively) contain allowable subject matter. Therefore, Applicant respectfully submits that claims 1 and 3 (which now incorporate the recitations of previous claims 27 and 28) are allowable *at least* by virtue of the Examiner's previous indication of allowable subject matter.

Second, without conceding to the merits of the Examiner's rejections, claim 1 has been amended, as set forth above, to recite (among other things):

...at least one first block receiving a  
variable supply voltage, said at least one first  
block receiving a clock signal;  
at least one second block receiving the  
variable supply voltage...

wherein the clock signal received by the at least one first block is different from a clock signal received by the at least one second block.

Support for the above amendments is provided by *at least* page 17, lines 9-10 and FIG. 6 of the original specification. No new matter has been added.

The grounds of rejection allege that Uchida's voltage generator 200 corresponds to the claimed variable supply voltage. The grounds of rejection also allege that Uchida's delay gates 223-226 correspond to the claimed "first block," and that Uchida's internal clock generator 121 corresponds to the claimed "second block," respectively. Applicant respectfully disagrees.

Uchida fails to disclose or suggest that the internal clock generator 121 receives the variable supply voltage from the voltage generator 200. Quite to the contrary, Uchida discloses that the output from the voltage generator 200  $V_O$  is supplied to the transistor 230 that supplies a current only to the delay gate array 220 (column 9, lines 52-64; FIG. 13). Uchida fails to provide any disclosure or suggestion whatsoever regarding supplying the output from the voltage generator 200  $V_O$  to the internal clock generator 121.

Moreover, there would have been no reason for one of ordinary skill in the art to modify the teachings of Uchida to achieve the claimed invention. Indeed, the object of Uchida is to control the output voltage from the voltage generator 200 to the delay gate array 220 so as to control the delay produced by the delay gate array 220 (column 1, lines 38-46). There would have been no suggestion for one of skill in the art to further modify Uchida so as to (among other things) supply the output from the voltage generator 200  $V_O$  to the internal clock generator 121.

Therefore, claim 1 is patentable over the cited Uchida reference for *at least* these reasons. Further, the dependent claims 2, 18 and 19 are patentable *at least* by virtue of their dependency.

In view of the similarity between the requirements of amended claim 3 and the requirements discussed above with respect to independent claim 1, Applicant respectfully submits that arguments analogous to the foregoing arguments as to the patentability of independent claim 1 demonstrate the patentability of claim 3. As such, it is respectfully submitted that claim 3 is patentably distinguishable over the cited reference *at least* for reasons analogous to those presented above. Further, Applicant submits that the dependent claim 29 is allowable *at least* by virtue of its dependency on claim 3. Thus, the allowance of these claims is respectfully solicited of the Examiner.

**VI. Claim Rejections Under 35 U.S.C. § 103**

Claim 22 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Uchida (US 5,926,046). Applicant respectfully traverses this rejection.

First, as acknowledged by the Examiner in the 10/16/08 Office Action, and the interviews conducted on December 30 and 31, 2008, claim 22 contains allowable subject matter. Therefore, Applicant respectfully submits that claim 22 is patentable over Uchida *at least* by virtue of the Examiner's previous indication of allowable subject matter.

Second, the Examiner acknowledges that Uchida fails to teach or suggest the features of wherein said voltage level detector circuit comprises a differential amplifier into which the supply voltage and a reference voltage is input, as claimed. Thus, the Examiner's rejection of claim 22 relies on the conclusory allegation that it is obvious that the complicated level detector 200 of Uchida can be replaced with a simpler circuit such as a diode or a differential amplifier having an input voltage.

However, the grounds of rejection do not provide any support whatsoever for this conclusory allegation<sup>1</sup>. Indeed, the Examiner's rejection of claim 22 on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness<sup>2</sup>. Since the grounds of rejection have not articulated any reasoning with some rational underpinning to support the conclusion that element 200 of Uchida can be replaced with a differential amplifier to achieve the recitations of claim 22, nor have they articulated any reason why one of ordinary skill in the art would have been motivated to do so, the current rejection of claim 22 is improper for *at least* these reasons.

Third, element 200 of Uchida is a voltage generator and not a complicated level detector, as alleged by the grounds of rejection. As taught in Uchida, the voltage generator 200 consists of a resistor 210 and n-channel MOS transistors 211 to 214 having different sizes (column 8, lines 53-63; FIG. 13). Uchida teaches that the control electrodes of the transistors 211 to 214 receive the voltage signals  $\phi 1$  to  $\phi 4$ , respectively, from the phase comparator 31 (column 8, lines 53-63; FIG. 13). Further, Uchida specifically teaches that the differences among the ON resistance values in the voltage generator 200 according to the output signals  $\phi 1$  to  $\phi 4$  determine the delay controlling resolution (column 9, lines 46-48).

There would have been no reason for one of ordinary skill in the art to fundamentally modify the specific configuration taught in Uchida to replace the voltage generator 200 with a differential amplifier having a reference voltage, as alleged by the grounds of rejection. Quite to

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<sup>1</sup> It is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

<sup>2</sup> KSR Int'l Co. v. Teleflex, Inc., 127 S. Ct. 1727, 1741 (U.S. 2007).

the contrary, the modification proposed by the Examiner would change the principle of operation of Uchida and, therefore, the teachings of the cited references are not sufficient to render the claims *prima facie* obvious (MPEP § 2143.01).

Therefore, claim 22 is patentable over the cited Uchida reference for *at least* these reasons and Applicant respectfully requests that the Examiner withdraw this rejection.

## **VII. New Claims**

New claims 30-35 have been added and are fully supported by *at least* page 40, line 14 - page 42, line 2 and FIG. 39 of the original specification. No new matter has been added.

Applicant respectfully submits that new claims 30-35 are patentable over the cited references *at least* by virtue of the recitations set forth therein.

## **VIII. Conclusion**

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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